

REMARKS

Claims 21-27 are pending in the present application.

Claim Rejections-35 U.S.C. 103

Claims 21-27 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Frye et al. reference (U.S. Patent No. 5,534,465) in view of the Yamada et al. reference (U.S. Patent No. 5,864,178). This rejection is respectfully traversed for the following reasons.

The method for fabricating a semiconductor apparatus of claim 21 includes in combination "fabricating a semiconductor substrate having a first surface in which a semiconductor integrated surface is formed", the semiconductor substrate including "a conductive layer formed on the first surface thereof which is connected to the semiconductor integrated circuit and including a base member of insulating material arranged between the first surface and the conductive layer". Applicant respectfully submits that these features would not have been obvious in view of the prior art as relied upon by the Examiner.

Particularly, the Examiner has interpreted substrate 20 in Fig. 4 of the Frye et al. reference as the semiconductor substrate of claim 1. The Examiner has further interpreted wettable metal region 36, as formed on additional insulating layer 35 and on conductive layer 34 (see Fig. 2), as the conductive layer of claim 21. However, as may be readily understood in view of Fig. 4 of the Frye et al. reference, wettable metal

region 36 is not formed on a first surface of substrate 20, as would be necessary to meet the features of claim 21. Wettable metal region 36 is formed on additional insulating layer 35 (interpreted as the base member of the claims) and conductive layer 25. Particularly, thin oxide layer 30 and metal contacts 25 (see Fig. 2) are formed on the surface of substrate 20. Accordingly, the Frye et al. reference as relied upon by the Examiner, as taken with the Yamada et al. reference, fails to disclose or make obvious all the features of claim 21. Applicant therefore respectfully submits that the method for fabricating a semiconductor apparatus of claim 21 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 21-24 is improper for at least these reasons.

Claim 23 as dependent upon claim 21, further features that the base member and the seal member "are made of a same material having a same thermal expansion coefficient". Applicant respectfully submits that the prior art as relied upon by the Examiner does not disclose or make obvious these features.

The Examiner has interpreted additional insulating layer 35 in Fig. 4 of the Frye et al. reference as the base member of claim 21. Additional insulating layer 35 is described very generally in column 3, lines 34-35 of the Frye et al. reference as preferably polyimide. A thermal expansion coefficient is not specified for additional insulating layer 35 of the Frye et al. reference, or even remotely considered.

The Examiner has acknowledged that the Frye et al. reference does not include a seal member in a space between a semiconductor substrate and a connection

substrate. In order to overcome this acknowledged deficiency of the Frye et al. reference, the Examiner has asserted that the use of a sealing member would have been obvious in view of the teaching in column 1, line 36 through to column 2, line 7 of the Yamada et al. reference. With respect to claim 23, the Examiner has alleged that the Frye et al. reference in view of the Yamada et al. reference "shows wherein the base member and the seal member are made of a same material having a same thermal expansion (Yamada, Column 56, Lines 27-46 and Column 57, Lines 31-48)". Applicant respectfully disagrees for the following reasons.

Firstly, columns 1 and 2 of the Yamada et al. reference as generally relied upon by the Examiner do not specifically teach the use of a base member and a seal member being made of a same material and having a same thermal expansion coefficient. This particular portion of the Yamada et al. reference very generally considers coefficients of thermal expansion of a semiconductor chip and a wiring circuit board, not specifically a base member and a seal member as featured in claim 21.

Moreover, column 56, lines 27-46 of the Yamada et al. reference describes a first encapsulation resin layer 204 having a coefficient of thermal expansion of $40 \times 10^{-6} (^{\circ}\text{C}^{-1})$. This first encapsulation resin layer 204 is further described as including 100 parts by weight of fused silica as a filler. In contrast, column 57, lines 31-48 of the Yamada et al. reference describes a third encapsulation resin layer 206 having a coefficient of thermal expansion of $35 \times 10^{-6} (^{\circ}\text{C}^{-1})$. Also, the third encapsulation resin layer 206 is described as including 200 parts by weight of fused silica as a filler.

Accordingly, the corresponding encapsulation resin layers of the Yamada et al. reference as considered by the Examiner are not made of the same material and do not have the same thermal expansion coefficient, as alleged by the Examiner. Moreover, as pointed out above, additional insulating layer 35 in Fig. 4 of the Frye et al. reference is very generally described as preferably polyimide, whereby a thermal expansion coefficient is not specified or even remotely considered. One of ordinary skill therefore would have no motivation to modify additional insulating layer 35 of the Frye et al. reference to have any specific thermal expansion coefficient, or more particularly to have a thermal expansion coefficient that is the same as any other layers of the structure or the same as any of the layers in the Yamada et al. reference. This would appear to be especially clear since the various encapsulation resin layers in the Yamada et al. reference have different thermal expansion coefficients, and are not the same materials since the filler amounts differ. Applicant therefore respectfully submits that the method of claim 23 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claim 23 is improper for at least these additional reasons.

The method for fabricating a semiconductor apparatus of claim 25 includes in combination "forming a semiconductor integrated circuit on a first surface of a semiconductor substrate" and "forming a conductive layer on the first surface of the semiconductor substrate, the conductive layer being connected to the semiconductor integrated circuit and having an extended portion that extends onto a top surface of the

base member”.

Applicant respectfully submits that the method for fabricating a semiconductor apparatus of claim 25 would not have been obvious in view of the prior art as relied upon by the Examiner for at least somewhat similar reasons as set forth above with respect to claim 21. Particularly, additional insulating layer 35 in Fig. 4 of the Frye et al. reference interpreted as the conductive layer of claim 25, is not formed on a first surface of substrate 20. Applicant also respectfully submits that claims 26 and 27 would not have been obvious in view of the prior art as relied upon by the Examiner for at least somewhat similar reasons as set forth above with respect to claim 23. Accordingly, Applicant respectfully submits that the method for fabricating a semiconductor apparatus of claim 25 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 25-27 is improper for at least these reasons.

Conclusion

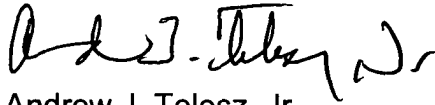
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.

A handwritten signature in black ink, appearing to read "A. J. Telesz, Jr.", written in a cursive style.

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